REMARKS

By this response claims 12 and 13 have been amended. Reconsideration of the application is respectfully requested. Claims 1-17 and 21-23 remain pending.

Rejections under 35 USC §102(e)

Claims 1-5, 8, 10-13, and 15-17 have been rejected under 35 USC §102(e) over Chiang et al., US Pat. 6,383,863. Chiang recites the formation of a semiconductor device in which a polycide layer 20 is simultaneously formed over a polysilicon transistor gate 4 and a capacitor top plate 18.

The present invention as claimed comprises novel and nonobvious differences over Chiang. Claim 1, for example, recites "...etching the at least one dielectric layer and the first conductive layer...to form first and second cross-sectional sidewalls from the at least one dielectric layer and the first conductive layer [and] forming a first dielectric spacer on the first sidewall and a second dielectric spacer on the second sidewall, wherein an upper surface of each sidewall is above an upper surface of the first and second spacers."

The Examiner uses layers 4 and 6 of Chiang as the conductive layer and the at least one dielectric layer respectively, and layer 11 to teach the first and second spacers of the claimed invention. Line 13 of paragraph [0017] of the present specification recites that "the term 'on' used with respect to two layers, one 'on' the other, means at least some contact between the layers". Because the present claim recites etching the dielectric layer and the first conductive layer to form first and second cross-sectional sidewalls, then forming the spacers "on" the sidewalls which, as defined in the specification, requires at least some contact, Chiang fails as a reference under 35 USC §102(e), at least because layer 11 does not contact the sidewall formed by layers 4 and 6. Layer 11 is separated from layers 4 and 6 by layer 10.

Further, the Examiner states that "an upper surface of each sidewall is above an upper surface of the first and second spacers (col 3 lines 37-39; fig. 4)." It should be noted that layer 11 as depicted in FIG. 4 has not been etched to form a spacer, and the recitation of the first and second spacers has thus not been met. Layer 11 *is* etched to form a spacer, for example as depicted in FIG. 8, however the upper surface of the sidewall provided by conductive layer 4 (dielectric layer 6 has been etched removed at this point) still is not above an upper surface of the spacer provided by FIG. 11.

Claim 1 further recites "...forming a second conductive layer over the at least one dielectric layer and over the first conductive layer; removing the second conductive layer from over the first conductive layer; then forming a silicide layer simultaneously on the first and second conductive layers." The Examiner uses capacitor top plate 18 as the second dielectric layer. As depicted in FIG. 6, top plate 18 is not removed from over conductive layer 4, but still has a significant portion overlying layer 4. It appears that over 30% of layer 4 is covered by layer 18. This results in only a portion of layer 4 being silicided, as may be determined from FIG. 10 in which only a portion of the layer 4 structures adjacent layer 18 is silicided. See, for example, the two layer 4 portions interposed between capacitor top plate 18 and bit line contact structure 19, which comprise silicidation over less than half of their width. Because the silicidation increases conductance, forming the material over the entire width of the conductive feature is desirable, and would appear to be performed by Chiang if possible. Thus the recitation from claim 1 of "removing the second conductive layer from over the first conductive layer" which results in the silicidation of the first conductive layer over its entire width (see FIG. 8 of the present invention, for example) is useful, novel, and nonobvious over Chiang.

With regard to claim 5, claim 1 recites "forming a first conductive layer and at least one dielectric layer on the first conductive layer...[and] etching the at least one dielectric layer and the first conductive layer...to form first and second cross sectional sidewalls from the at least one dielectric layer and the first conductive layer." Claim 1 further recites forming a first spacer on the first sidewall and a

second spacer on the second sidewall. Claim 5 recites that the formation of the at least one dielectric layer comprises "forming a first silicon dioxide layer, forming a silicon nitride on the first silicon dioxide layer; and forming a second silicon dioxide layer on the silicon nitride layer." Thus the at least one dielectric layer, which comprises the first and second silicon dioxide layers and the silicon nitride layer, is formed and etched, then the spacers are formed on the sidewalls. Chiang further fails as a reference under 35 USC §102(e), at least because Chiang teaches forming conductive layer 4, silicon oxide 5, and silicon nitride 6, then etching layers 4, 5, and 6, and then forms silicon oxide layer 10 on the sidewalls of layers 4, 5, and 6.

Claim 10 recites "...providing a blanket polysilicon word line layer and at least one dielectric layer on the word line layer; using a single mask, etching the word line layer and the at least one dielectric layer to define a plurality of transistor word lines; forming a blanket polysilicon plug layer over the plurality of transistor word lines and over the at least one dielectric layer; planarizing the blanket polysilicon plug layer to remove the plug layer from over the plurality of transistor word lines to form a plurality of polysilicon plugs and to expose the at least one dielectric layer...".

The Examiner uses the polysilicon word line layer 4 and the dielectric layer 12 of Chiang to teach the polysilicon word line layer and the at least one dielectric layer of claim 10. Claim 10 is allowable over Chiang as applied by the Examiner at least because layer 12 is not "provided...on the word line layer" as defined relative to the present specification at line 13 of ¶[0017], that is there is no contact between layer 4 and layer 12. Even if layer 5, which contacts layer 4, and layers 6, 10, 11, and 12 are used as the "at least one dielectric layer" of claim 10, these five layers are not etched "to define a plurality of transistor word lines." Layers 5 and 6 are etched during the definition of word line between FIGS. 1 and 2 of Chiang, but layers 10-12 are not present during this etch.

Further, the Examiner uses the material of layer 19 and the text at col. 4 lines 25-40 to teach "planarizing the blanket polysilicon plug layer to remove the plug layer from over the plurality of transistor word lines to form a plurality of polysilicon plugs and to expose the at least one dielectric layer." However, at the indicated text location, Chiang recites masking and etching the material of layer 19, not planarizing the layer. This layer is not planarized, for example because the upper surface of layer 18, the capacitor top plate, and the upper surface of layer 19, the bit line contact structure, are at different levels. Chiang indicates that one layer and one mask is used to provide these two different structures (col. 4 lines 31-36). Further, the etch of the layer which forms structures 18 and 19 does not "expose the at least one dielectric layer." The Examiner uses layer 12 as the "at least one dielectric layer," and this layer is not exposed during the etch of layer 18.

With regard to claim 11, the Examiner uses layer 12 in claim 10 to teach the "at least one dielectric layer" and also uses the same layer 12 to teach "subsequent to etching...the at least one dielectric layer, forming a plurality of dielectric spacers on the plurality of transistor word lines." This does not appear to be a reasonable application of layer 12, as it requires layer 12 to be etched before it is actually formed (the at least one dielectric layer is etched before formation of the spacers), then formed after it is etched (the spacers are formed on the word line after the word line and the at least one dielectric layer are etched). This interpretation of layer 12 is possible only in hindsight using the present claims as a blueprint, which is impermissible (*Interconnect Planning Corp. v. Feil,* 774 F.2d 1132, 227 USPQ 543, Fed. Cir. 1985). Thus the Examiner's use of layer 12 to teach both the "at least one dielectric layer" and the "plurality of dielectric spacers [formed] on the plurality of transistor word lines" is respectfully traversed.

Claim 12 recites "forming a first sidewall and a second sidewall from...the at least one dielectric layer during the etch of the...at least one dielectric layer; and forming the plurality of dielectric spacers on the plurality of transistor word lines, wherein the first and second sidewalls extend beyond an upper surface of each spacer." As the Examiner uses dielectric layer 12 to teach both the "dielectric

spacers" which extend beyond an upper surface of each sidewall and the "at least one dielectric layer" which forms part of the sidewall, this would appear to improperly use the present claims as a blueprint for the application of layer 12 of Chiang.

Claim 13 has been amended and is further allowable over Chiang under 35 USC §102(e), which fails to teach or suggest "exposing a vertically-oriented portion of each spacer during the removal of the at least one dielectric layer; and forming the metal layer on the vertically-oriented portion of each spacer during the formation of the metal layer."

Claim 15 comprises novel and nonobvious differences over Chiang. Claim 15, for example, recites "...removing a portion of the blanket conductive plug layer by planarizing the blanket conductive plug layer in the absence of a mask layer to form a plurality of conductive plugs." The Examiner states that this is taught by Chiang at col. 4 lines 35-40. However, the cited location recites that a "photoresist shape, not shown in the drawings is formed and used as an etch mask to allow a selective, anisotropic RIE procedure using Cl_2 or SF_6 as an etchant for polysilicon, to define capacitor top plate structures 16, in capacitor openings 14a, and bit line contact structure 19, in bit line opening 14b." Thus Chiang expressly recites the use of an etch mask at the text location specified by the Examiner. Planarizing the blanket polysilicon layer does not appear possible with Chiang, at least because it would result in a disconnect of the top plate of each capacitor from all other capacitors in the array. Therefore, Chiang's process requires a pattered mask which is known in the art to be avoided where possible so that mask misalignment and device costs may be reduced (see, for example, ¶[0007] of the present application). Thus claim 15 is allowable over Chiang under 35 USC §102(e) for at least this reason.

Claim 16, in combination with claim 15, recites "forming a first silicon dioxide layer, a silicon nitride layer, and a second silicon dioxide layer [on the transistor word line layer] during the formation of the blanket dielectric layer [and] ...patterning the blanket dielectric layer and the blanket conductive transistor word

line layer using the patterned mask to form a patterned dielectric layer from the blanket dielectric layer and a plurality of transistor word lines from the blanket conductive word line layer." The Examiner uses layer 5 of Chiang as the first silicon dioxide layer, layer 6 as the silicon nitride layer, and layer 10 as the second silicon dioxide layer. The two dielectric layers of Chiang, silicon dioxide 5 and silicon nitride 6 which are patterned between FIGS. 5 and 6 form blanket layers which are patterned during the etch of the word lines, but layer 10 is formed subsequent to patterning of the word lines, and after removal of the resist 8 which patterns layers 4, 5, and 6. Chiang goes on to form and pattern layer 10, but not until after patterning the blanket dielectric layer (comprising layers 5 and 6) and the word lines. Thus layer 10 cannot be considered part of the blanket dielectric layer of the present invention as claimed, as it is not etched during the patterning of the word lines.

Claim 17 recites "...forming first and second dielectric spacers on the patterned dielectric layer and on the transistor word lines such that an inside surface of each spacer contacts the patterned dielectric layer and wherein the patterned dielectric layer extends above a top of each of the first and second dielectric spacers; exposing the inside surface of each of the first and second spacers during the removal of the patterned dielectric layer...". The Examiner states that this is disclosed by Chiang and refers to FIGS. 4 and 8. Referring to the present specification, "on" with reference to the present invention requires at least some contact between the two layers (line 13 of ¶[0017]). While the Examiner does not indicate which layer is being used to teach the present spacers, layer 10 of FIG. 4 is the only layer which contacts the patterned dielectric layer 5, 6 and the transistor word lines 4. However, the patterned dielectric layer 5, 6 does not "extend above a top of each of the first and second dielectric spacers" as presently recited, but instead layer 10 overlies the top of the dielectric layers. Further, an inside surface of the layer 10 which contacts the word line is not exposed during the removal of the patterned dielectric layer (see FIGS. 7 & 8), but rather layer 10 is also etched such that the top of layer 10 is the same height as the top of the word line 4. The vertical portion of layer 10 located between top plate 18 and bit line 19 which is

exposed during the etch of dielectric layer 6 overlies dielectric layer 6, and thus does not fulfill the recitation that the "patterned dielectric layer extends above a top of each of the first and second dielectric spacers." Thus claim 17 is further allowable over Chiang.

Thus for the foregoing reasons, rejected claims 1-5, 8, 10-13, and 15-17 are allowable over Chiang as applied by the Examiner under 35 USC §102(e). The rejected claims not individually addressed are allowable at least because they depend from an allowable base claim.

Rejections under 35 USC §103(a)

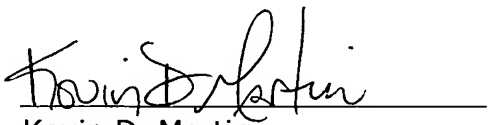
Claims 9 and 14 have been rejected under 35 USC §102(a) as being unpatentable over Chiang in view of Shin, et al. (US Pat. No. 6,635,536). Chiang recites the elements discussed relative to the rejections under 35 USC §102(e). Shin recites the formation of a spacer from silicon nitride or aluminum oxide (col. 2, lines 33-35).

Claims 1 and 10 from which claims 9 and 14 depend, and claim 11 from which claim 14 further depends, are allowable over Chiang for the reasons discussed relative to the rejections under 35 USC §102(e) above. Because Chiang in view of Shin fails to teach or suggest all the recitations of claims 1, 10, and 11 from which claims 9 and 14 depend as required (MPEP §706.02(j)), claims 9 and 14 are allowable over Chiang in view of Shin under 35 USC §103(a).

Conclusion

If there are matters which may be clarified or resolved through a telephone call, the Examiner is cordially invited to contact the undersigned. This is believed to be a complete response to the Examiner's office action.

Respectfully submitted,



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